

## High Frequency Circuit Materials Attributes

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Specialty high frequency circuit materials have been used in the PCB industry for decades and for many different reasons. There are several attributes of these materials that are very unique when compared to the more traditional PCB materials. When these attributes are well understood, PCB fabricators and OEMs can benefit greatly from improved electrical performance.

In addition there are many other non-electrical improvements that can be achieved, which the PCB industry audience may not be aware. In order to realize the full potential of the benefits these materials offer, PCB fabrication issues must be well understood.

Most high frequency applications will have multiple demands for PCB materials and not just one specific item of interest. For a specific application, many times one concern is paramount while others are secondary. Understanding these needs and the attributes of high frequency materials allows the user to choose the optimum material for the specific application at hand. A couple of application examples will demonstrate the various attributes to consider.

A simple application example could be a small filter circuit using high frequency materials that will be soldered to a larger FR4 circuit board, as shown in figure 1.

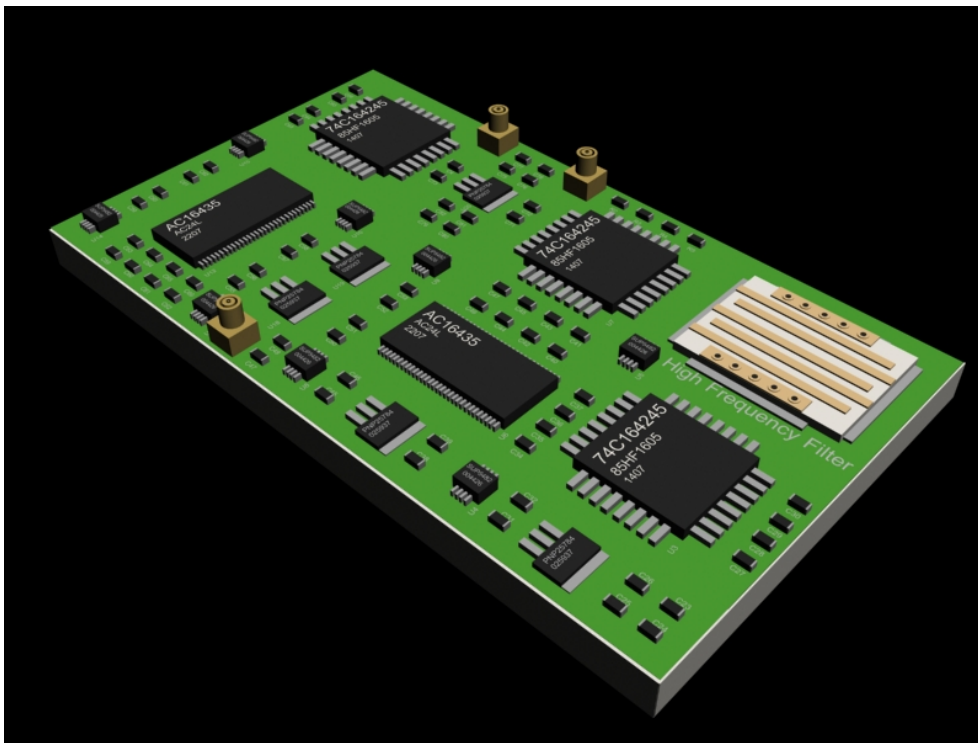


Figure 1. PCB with a high frequency filter

The completed assembly will be encased inside a sealed enclosure and will operate in an environment that will vary greatly due to outdoor seasons and equipment heat generation. Temperatures inside the enclosure could vary from  $-25^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ .

Filter circuits will typically need a material with very consistent dielectric constant (dk). This means consistent dk within a sheet of circuit material as well as from lot-to-lot. This is required so the filters being attached to the FR4 circuits will have the same performance and minimal tuning will be necessary. This filter will be a double-sided (2 copper layer) plated through-hole (PTH) circuit, with a ground plane on the bottom and the signal plane on top; microstrip edge coupled filter. As previously mentioned, most high frequency applications have more than one demand on these circuit materials. In this case the consistent dk is paramount, but there are other demands that are implied and not specified yet.

All circuit materials have some amount of growth / shrinkage due to heating / cooling of the material. That is due to the coefficient of thermal expansion (CTE) of the material. In this case the CTE may not appear to be important, but it can be critical. Once the filter is soldered in place to the FR4, the solder joints are a rigid bridge between the FR4 circuit and the high frequency filter.

When the unit experiences a change from  $0^{\circ}\text{C}$  to  $+30^{\circ}\text{C}$  (as an example), then the FR4 and the filter circuit will want to expand. If the CTE is significantly different between the FR4 and the filter, stresses can develop at the solder interface, which connects them. In this example, if it was only one excursion from  $0^{\circ}\text{C}$  to  $+30^{\circ}\text{C}$  then it may not be a problem. However if it is a dynamic environment where it will cycle up and down  $0^{\circ}\text{C}$  and  $+30^{\circ}\text{C}$ , this will cause an accordion affect with the different materials growing and shrinking in different amounts and can shear off the solder that connects them.

Another possible critical issue that may not be apparent for this application is the TCdk of the circuit material. Each type of circuit material has a property where the dk value can change with a temperature change, and that is the thermal coefficient of dielectric constant or TCdk. So with a certain circuit material the dk may appear to be good and consistent when tested at room temperature – however, in the application, and as the temperature changes, then the dk can change and cause the filter to perform significantly different.

An additional consideration could be the assembly operation, where the filter is soldered to the FR4 circuit board. Since the filter has plated through-hole via's, the z-axis (thickness) CTE could be a concern during the soldering operation. Depending on the design of the filter and / or the FR4 circuit there may be a need to dwell at elevated soldering temperatures for a longer period of time. If the circuit material has a higher z-axis CTE, then the dwell at elevated temperatures can cause damage to the plated through-hole via's and degrade the electrical connection from the signal plane to the ground plane.

Lastly, if the filter is intended to operate over a wide range of frequencies, most circuit materials will have different dk values at different frequencies. Some materials are more stable than others, but this may also need to be considered.

In summary for this application example, this filter circuit should use a material that has a tight tolerance for dk, a CTE that is closely matched to FR4 in the x-y plane, a low TCdk, a low z-axis CTE and a stable dk vs. frequency curve. There are many high frequency circuit materials to choose from but finding the right circuit material, which fills all of these requirements, will reduce the available choices. A comparison between the properties of a standard FR4 circuit material and the material under consideration for the best choice is highly recommended. For this example, the typical values regarding the properties of interest for a standard FR4 material are shown in figure 2. The user will need to determine the fitness for use of the selected materials by conducting appropriate short-term and long-term reliability testing as dictated by the needs of the application.

	x-y axis CTE (ppm/C)	z axis CTE (ppm/C)	TCdk (ppm/C)
Standard FR4	15	65	300

Figure 2. Typical values for a standard FR4 material

Additionally, if it was critical to reduce the physical size of the filter then a different circuit material may have been chosen with a high dielectric constant. A material with high dielectric constant will allow the circuit to be reduced in size and still perform the same function. Also, the high frequency circuit material used for this filter may not have been used at a relatively high frequency. The material may have been used due to the tight dk values and the other properties mentioned.

Another area where most high frequency materials have advantage over traditional PCB circuit materials is minimal moisture absorption. Having low moisture absorption is important for several reasons and for high frequency applications it is consistent dk. Water has a dk value of about 70 and even a small amount of moisture absorbed into a high frequency circuit or a controlled impedance circuit can change the electrical performance.

Another application example will be a microstrip circuit, which will need to be formed to a specific shape around a mandrel that is 1/2" diameter. The electrical concerns are primarily low insertion losses (< 0.05 dB/in), tightly controlled impedance (50 ohms +/- 5%) and operation at 900 MHz. Typically an application operating at 900 MHz is not considered high frequency and more traditional PCB materials could normally be used. Yet considering the electrical concerns, there are several reasons why a high frequency grade material should be used.

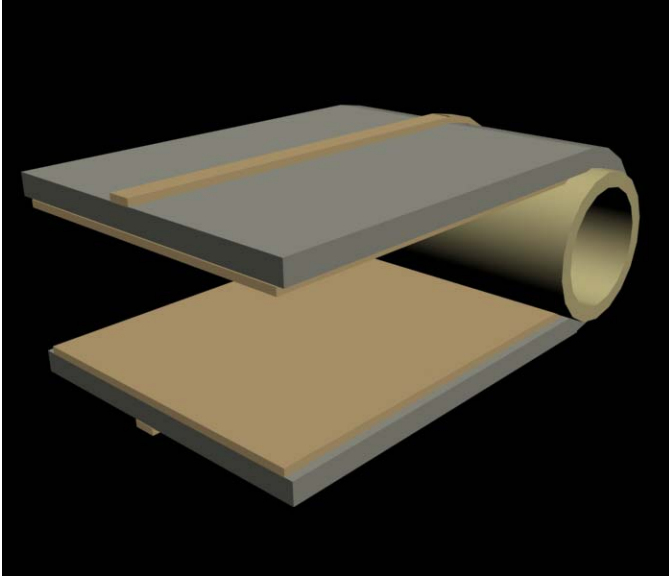


Figure 3. Second example of a simple microstrip, bent around a mandrel

The need for tightly controlled impedance translates to a substrate that must have tightly controlled thickness and  $dk$  values. Traditional PCB materials will not control these attributes near as well as high frequency circuit materials. Of course the etching control of the conductor width will need to be very well controlled at the circuit fabricator as well.

The concern of low insertion loss, overall, can be rather complicated. There are many issues that can affect this circuit property, and the following are a few items that can be a concern: connectors, signal launch design, plating finish on the copper conductors, dissipation factor of the substrate, copper roughness, circuit geometry and some assembly processes. When choosing the material that will give the best advantage for insertion loss, a material with a low dissipation factor, smooth copper, and low moisture absorption would be optimum. Also, the circuit design should use a relatively thick substrate.

In this case there are concerns of a mechanical nature and forming a circuit around a mandrel. Typically a thinner substrate, with no glass reinforcement, will be better for forming the circuit and generating less stress on the copper layers. Also the copper type should be rolled wrought or rolled annealed copper, which has a grain structure that is optimum for elongation in the x-y plane [1].

One more consideration could be the type of plating finish to apply to the copper conductors of the microstrip. If enig (electroless nickel / immersion gold) were used, then the nickel is brittle and can be problematic for bending. The enig process will also typically deposit a thickness of approximately 100 to 200 microinches of nickel and around 10 microinches of gold. With the operating frequency at 900 MHz, the skin effects will force the signal to use about 87 microinches of conductor. That means the signal energy will predominately use the nickel layer, and nickel will cause an increase in

conductor losses and ultimately insertion losses. This is due to the fact that nickel is less conductive than copper and that it has a permeability value that is much greater than copper. The permeability value will adversely affect the magnetic fields of the propagating waves.

In summary, this application should use a high frequency material that has a tight control of the dk and thickness tolerance, low dissipation factor, smooth copper, non-glass reinforced, low moisture absorption and a non-nickel/gold finish. To determine the optimum thickness there will need to be a trade-off between mechanical and electrical properties. For a one-time bend there is a rule of thumb that states the stress on the copper should be approximately 2% or less. Figure 4 shows a comparative table of different materials and thicknesses relative to the mechanical stress values and insertion losses.

Model Order	Material	Thickness (in.)	Dielectric Constant (dk)	Dissipation Factor (df)	Conductor width 50 ohm (in.)	Mechanical Stress (%)	Insertion Loss (dB/in.)
1st	RO3003™	0.030	3.00 +/- 0.04	0.0013	0.075	7.583	0.0216
2nd	RO3003™	0.010	3.00 +/- 0.04	0.0013	0.025	2.335	0.0576
3rd	RT/duroid®	0.010	2.20 +/- 0.02	0.0009	0.030	2.375	0.0335

Figure 4. Comparison between different materials and thickness

In figure 4 it can be seen from the 1<sup>st</sup> model to the 2<sup>nd</sup> that the thickness of the substrate decreased. The decrease in thickness improved the mechanical stress significantly. A decrease in the substrate thickness will force a decrease of the conductor width in order to maintain 50 ohms. The decreased conductor width will increase the conductor loss and ultimately the insertion loss.

When going from the 2<sup>nd</sup> to the 3<sup>rd</sup> model a different material was selected. This had a lower dielectric constant and lower dissipation factor while maintaining the same substrate thickness. The lower dielectric constant would dictate an increase in conductor width to maintain 50 ohms. The increase in conductor width will lower conductor losses. And the decrease in dissipation factor will lower dielectric losses. With lower conductor and dielectric losses, insertion loss will also decrease.

It can be seen that the stress number is a little higher than would be desired, but when looking at other models this appears to be the best-case scenario. In reality this may be good for the actual application, and, if not, then the diameter of the mandrel would need to increase some to lower the stress.

Some times there are interactions between the high frequency circuit materials and the PCB fabrication process, which can affect the circuit performance for the end user. Understanding the PCB fabrication concerns for these materials can be important for the end user. However, it can be even more important for the circuit fabricator in order to achieve good manufacturing yields along with a quality and highly reliable finished circuit. Each type of high frequency materials has their own unique circuit fabrication concerns.

The following discussion will focus on the fabrication concerns for the most common high frequency materials. These materials are: PTFE (Teflon<sup>®</sup>), PTFE with ceramic fillers, and non-PTFE thermoset resin systems with ceramic loading. Also the bonding materials that can be used to make multilayers from these materials will be discussed. Following will be information regarding LCP (Liquid Crystalline Polymer) materials, which are less commonly used and offer very unique properties to enable new evolving PCB applications. Lastly, some hybrid circuit constructions will be discussed.

The high frequency circuit materials that have been used in the industry for the longest period of time are the PTFE materials. Most of these materials are not pure PTFE but will have some small amount of micro-fiber glass impregnated into the substrate or will be PTFE with woven glass reinforcement or possible ceramic filled. In general, and in comparison to the other types of high frequency materials, the nearly pure PTFE without woven glass can be the most challenging type of circuit material to use in PCB fabrication.

There are several reasons for this: PTFE has a high CTE; PTFE doesn't allow adherence of other materials easily, and the PTFE substrate is soft and can be easily distorted. From an electrical performance perspective, however, PTFE substrates are typically the best to use. The ceramic filled PTFE substrates are typically much easier for PCB fabrication.

The main issues for the PCB fabricator to know about for PTFE circuit fabrication are: drilling without any smear, never scrub or mechanically alter the substrate, dimensional stability (scaling) issues will have to be fine tuned and possibly adjusted on every panel, very good practices to minimize handling damage of the soft substrate are critical, using a special through-hole wall preparation process is needed to allow the copper plating to adhere to the PTFE drilled material, and an understanding of how to laminate PTFE materials with other bonding materials.

There are no known processes that can de-smear PTFE, so when drilling the material it is of paramount concern to minimize heating and ensure there is no smearing of the substrate. General parameters for drilling PTFE substrates are shown in figure 5.

	Nearly Pure PTFE	Ceramic filled PTFE
Entry Material	Phenolic	Phenolic
Exit Material	Phenolic	Phenolic
Drill tool	Carbide	Carbide
Infeed	1-2mil/inch	2-3mil/inch
SFM	150-250	200-300
Retract rate	<500 inch/min.	<500 inch/min.
Drill life	~500-750 hits	~250-500 hits

Figure 5. Drilling parameters for PTFE substrates

The drill tool should be new and not a re-sharpened tool for the nearly pure PTFE. This is to make sure that the cleanest possible cut in the material can be made without smearing. However, a re-sharpened tool can be used for ceramic filled PTFE substrates. If the circuit board is a hybrid using PTFE and other non-PTFE materials, then the drilling conditions should always be adjusted for the best PTFE drilling conditions. And if hybrid and there is only one outer layer of PTFE, then the circuit should be drilled with the PTFE up (toward drill tool entry).

After the holes have been drilled, the PTFE material will need to be prepared for activation so the copper plating process can achieve a good copper plated through hole. In the case of the nearly pure PTFE substrates, a wet chemistry process is recommended prior to the copper plating process. This process will use sodium naphthalene (or some derivative), which will strip a fluorine atom in order to make the PTFE substrate wettable and accept the copper plating. There are companies that supply this service and two of them are shown below with their contact information.

Poly-Etch®  
 Matheson Gas Products  
 61 Grove St  
 Gloucester, MA 01930  
 978/283-7700  
 Fax: 978/283-6177

™Fluoro-Etch®  
 Acton Associates, Inc  
 100 Thompson St  
 Pittston, PA 18640  
 570/654-0612  
 Fax: 570/654-2810

For ceramic filled PTFE substrates the same wet process treatment can be applied but there is a caution that a thorough bake must be done on the panels just prior to the copper plating. The ceramic filled PTFE substrates can absorb some of wet processing chemistry. If these chemistries are not baked out prior to sealing in the material with a PTH, then in later processes that are at elevated temperatures the entrapped chemistry will volatilize and cause delamination of the substrate. A safer process for the ceramic filled PTFE substrates would be the use of a special plasma cycle that can make the substrate wettable and accept plating chemistries. There are two plasma cycles that are commonly used. The parameters for the first plasma cycle are shown in figure 6.

Gasses	NH <sub>3</sub> or (70% H <sub>2</sub> / 30% N <sub>2</sub> )
Pressure	100 mTorr Pump-down
Gasses	250 mTorr Operating
Power	4000 Watts
Frequency	40 KHz
Voltage	500 - 600 Volts
Cycle Time	10 - 30 minutes

Figure 6. Recommended plasma cycle for Ceramic filled PTFE substrates.

The second plasma cycle is similar to the first with all conditions except the type of gas that is used. In this case the gas would 100% Helium.

There are several materials that can be used as a bonding medium for multilayer PTFE circuits. Actually most bonding materials used in the PCB industry can be used as a bonding layer for a multilayer PTFE circuit, with some precaution. The main point of interest would be not to alter the exposed substrate surface. After the copper etching process the exposed PTFE substrate surface should not be mechanically altered in any way. The mirror image of the copper profile, from the copper that was etched away, will be the surface roughness of the exposed PTFE. This surface will need to remain unaltered in order to assist with some mechanical bonding with the bonding material.

A scrubbing process will actually polish the soft PTFE surface and have an adverse affect on the bonding. And it is not necessary to perform a process on the exposed PTFE substrate to activate it in order to accept a bonding material. There is a benefit to performing a bake cycle for the ceramic filled PTFE just prior to lamination. The bake cycle is intended to drive off any possibly absorbed processing chemistry and can be done at 121°C (250°F) for 1 to 2 hours. The recommended processing parameters for the particular bonding material should be followed.

The choice of bonding materials is a mixed decision between circuit fabrication issues and end use performance. If the bonding layer is a substrate layer that is not electrically important, then standard FR4 bonding materials can be used. If the layer is electrically important then a more high performance bonding material should be used. There are several bonding materials to choose from and in figure 7 there is information which highlights the electrical characteristics as well as some key fabrication issues for several high performance bonding materials.

Bonding Material	Dielectric Constant	Dissipation Factor	Lamination Temperature (F)	Preparation for PTH	Re-melt Temperature (F)
FEP	2.10	0.0010	565	Special	520
RO3003™	3.00	0.0013	700	Special	640
RO3006™	6.15	0.0020	700	Special	640
ULTRALAM® 3908	2.90	0.0025	554	Special	520
3001	2.30	0.0030	425	Special	350
RO3010™	10.80	0.0023	700	Special	640
RO4450B™	3.90	0.0040	350	Standard	N/A
RO4450F™	3.90	0.0040	350	Standard	N/A
SPEEDBOARD® C	2.60	0.0040	440	Special	640
FR4	4.50	0.0180	360	Standard	N/A

Figure 7. A list of high performance bonding materials

The mentions of special preparation for PTH in figure 7 is in regard to making the substrate active to where it will accept copper plating, as previously discussed. The mention of a standard preparation relates to a standard permanganate or plasma cycle typically used for FR4 materials.

The reference of a re-melt temperature is for the thermoplastic materials that can reflow or melt in later processes at elevated temperatures. The re-melt could cause the multilayer to delaminate. If a soldering operation would need to be performed on the multilayer it should be lower than the re-melt temperature or the proper bonding materials selected to endure the soldering operation. The materials that have an “N/A” are thermoset and will not melt or reflow in subsequent processes.

Another family of high frequency materials would be the non-PTFE materials. These materials are basically a resin system with some filler and / or additive, which allows the materials to perform well at higher frequencies. Typically these materials are easier for PCB fabrication; however, they do not have the superior electrical performance of PTFE.

The materials that are a resin system with ceramic filler have unique demands for the fabricator. These demands do not require different equipment than what is needed to process FR4 materials, but different parameters for this equipment are often necessary. The following is a brief highlight of the important fabrication issues regarding ceramic loaded resin systems: drill tool life is low, drill tools should not be re-sharpened or reused, rough drilled hole wall quality, loose ceramic particles after through hole wall preparation, prepreg’s have minimal flow characteristics and the prepreg’s are sensitive to low pressure areas during lamination.

Drilling the ceramic filled resin systems is more like excavating as opposed to drilling. At the through hole wall the drill tool will either remove the ceramic particle or let it remain. This makes for a rough drilled hole-wall which is actually better for plated copper adherence. Drilling the ceramic loaded materials will damage the drill tool quickly as well as the flute, and this is why the drill tool should not be reused. The starting drill parameters for this type of material are shown in figure 8.

Surface Speed	300 - 500 SFM
Chip Load	0.002" - 0.004"/rev.
Retract Rate	500 IPM
Tool Type	Standard Carbide
Tool Life	2000 hits

Figure 8. Drilling parameters for non-PTFE ceramic filled resin systems.

Where minimizing heat to eliminate smear with PTFE is very important, that is not the case with ceramic filled resin systems. Of course it is best to have drilling conditions that yield a good quality through hole and with minimal smear. These materials can be processed in permanganate or a standard FR4 plasma cycle for de-smear. The ceramic particles will not be affected by these processes, so it is necessary to have a high-pressure spray rinse after the de-smear process to remove any loose ceramic particles.

The prepreg's that are ceramic filled resin systems will typically have less flow and are sensitive to low pressure areas during lamination. The low-pressure areas are many times due to the design of the circuit, where there are many copper features aligned in the cross-section of the circuit. This means that the areas between "stacked" copper features will have lower pressure and this can cause the resin and ceramic particles to separate and not flow homogenously. The resin separation may have a different CTE than the homogenous prepreg and could have problems with solder or other elevated temperature exposures. To minimize this risk there are several items to consider: in the lamination process use a conformal material next to the panels, use highest pressure possible, at the beginning of the cycle have a hold for 20 minutes at the temperature where the prepreg will have the lowest viscosity and after which ramp up to the cure temperature. An example of a circuit with low-pressure areas and resin separation is shown in figure 9.

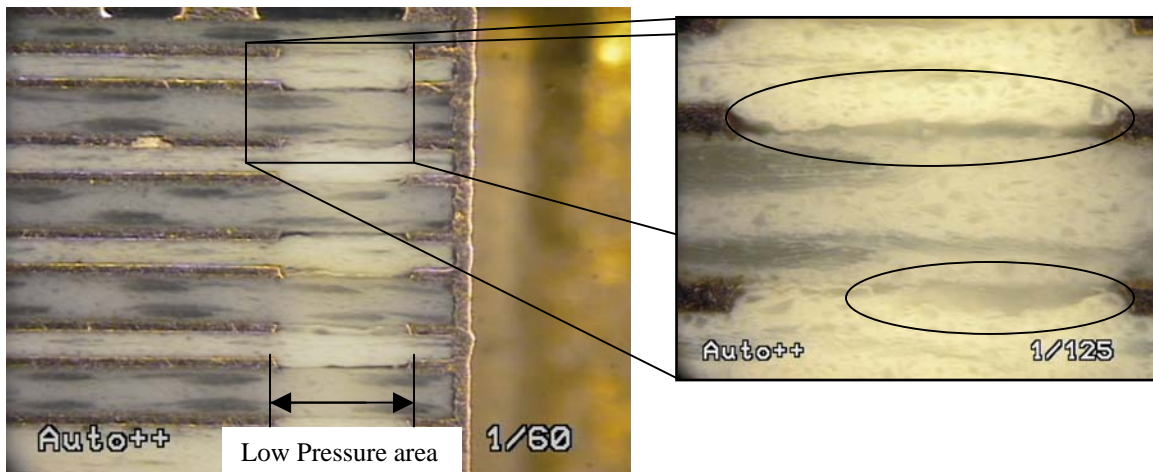


Figure 9. Cross-section of a circuit with a low pressure areas and resin separation circled.

One particular ceramic filled resin prepreg which was developed to specifically minimize or eliminate the resin separation issue is the Rogers RO4450F<sup>TM</sup>. Figure 10 shows a similar circuit using this prepreg.

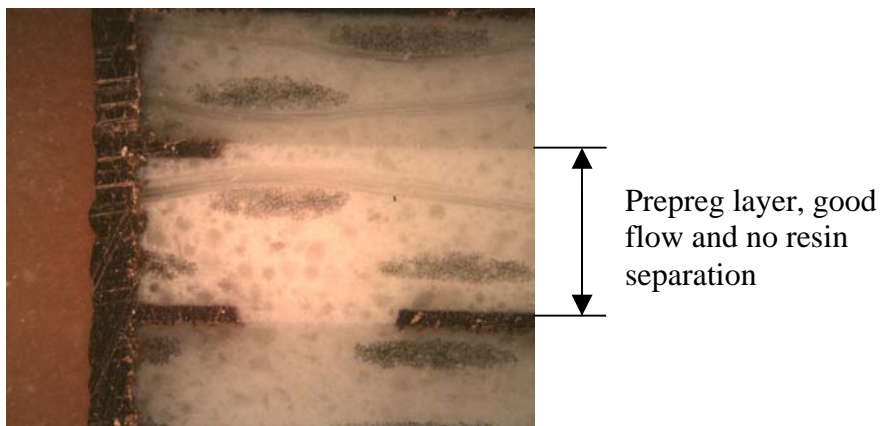


Figure 10. Cross-section of a circuit using RO4450F<sup>TM</sup> prepreg

LCP circuit materials offer many unique characteristics for multiple end-user applications. These materials have been available in the industry for a number of years. However, they are not well adopted by traditional PCB fabricators. The reason is due to unique processing requirements and the need for some processes to be extremely well controlled.

Some of the excellent properties of the LCP material are: halogen-free, consistent dk, low TCdk, dk vs. frequency is very good, low dissipation factor, dissipation factor vs. frequency is very good, very high frequency capable, extremely low outgassing, extremely low moisture absorption, no issue with CAF or electromigration, very high MOT (Maximum Operating Temperature) rating, nearly perfect hermetic sealed circuit possible, excellent chemical resistance, inert substrate and is naturally flame retardant.

An example of a coplanar waveguide tested over a very wide frequency band and with different LCP thickness is shown in figure 11.

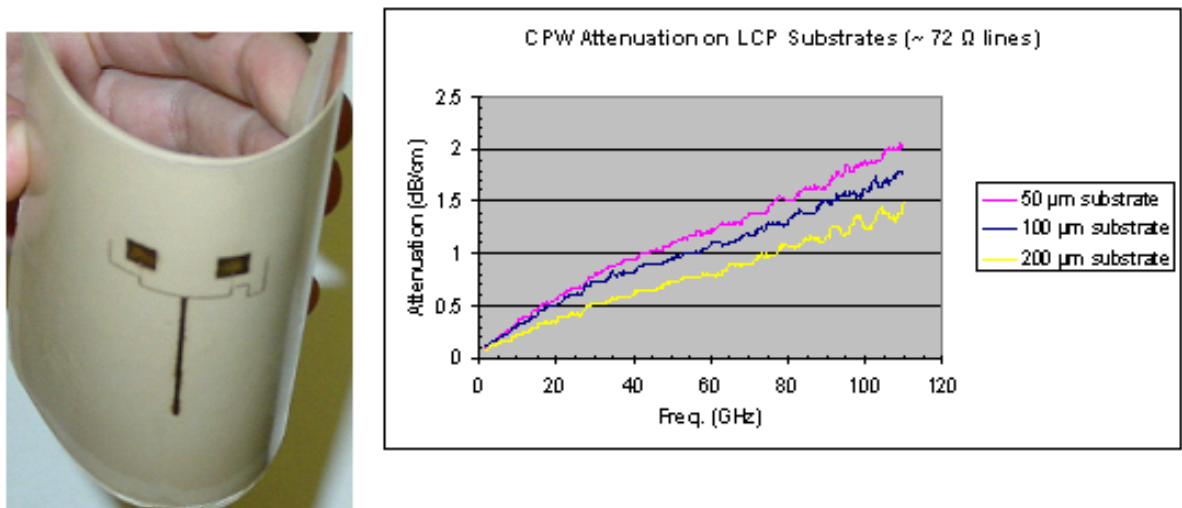


Figure 11. Flexible LCP circuit used as an antenna [2]

There are several fabrication issues, and a more detailed discussion can be found at: <http://www.rogerscorp.com/acm/products/17/ULTRALAM-3000-Series-Liquid-Crystalline-Polymer-Circuit-Materials.aspx>

In general the main issues regarding LCP fabrication are: thin and soft laminates, dimensional stability (scaling) issues like thin flexible circuit materials, special high temperature lamination for LCP multilayers, special PTH preparation is necessary, drilling is important to avoid smear, venting and border patterns are important.

The lamination for a pure LCP multilayer will require a high temperature lamination that is well controlled for temperature and pressure distribution. The lamination materials that will be used next to the actual circuit materials will need to be very conformal. Typically several sheets of skived Teflon<sup>®</sup> (2 or 3 sheets of 2mil Teflon<sup>®</sup>) are used as the lamination release and the conformal. Besides the conformal having the benefit of pushing the bond layer of the LCP into the circuit geometry, the conformal also helps to minimize any detrimental affect due to pressure distribution anomalies.

There will be some small amount of outgassing during the lamination cycle and since LCP is a very good vapor barrier, having venting holes and good border channels are important. For the inner layer circuit border pattern, a dot pattern should be used to ensure that there are complete venting paths to the outside edge of the circuit panel. These dot patterns should not align from layer-to-layer. The venting holes should be drilled through all layers, as many as possible and are non-PTH holes. Prior to the high temperature lamination the LCP materials should have had a good acid rinse and a bake at 121°C (250°F) for 4 hours.

The high temperature lamination cycle uses a dwell at 260°C (500°F) with low pressure and vacuum assist in order to help remove the outgassing prior to raising the pressure and temperature for the fusion bond cycle. This is shown in figure 12.

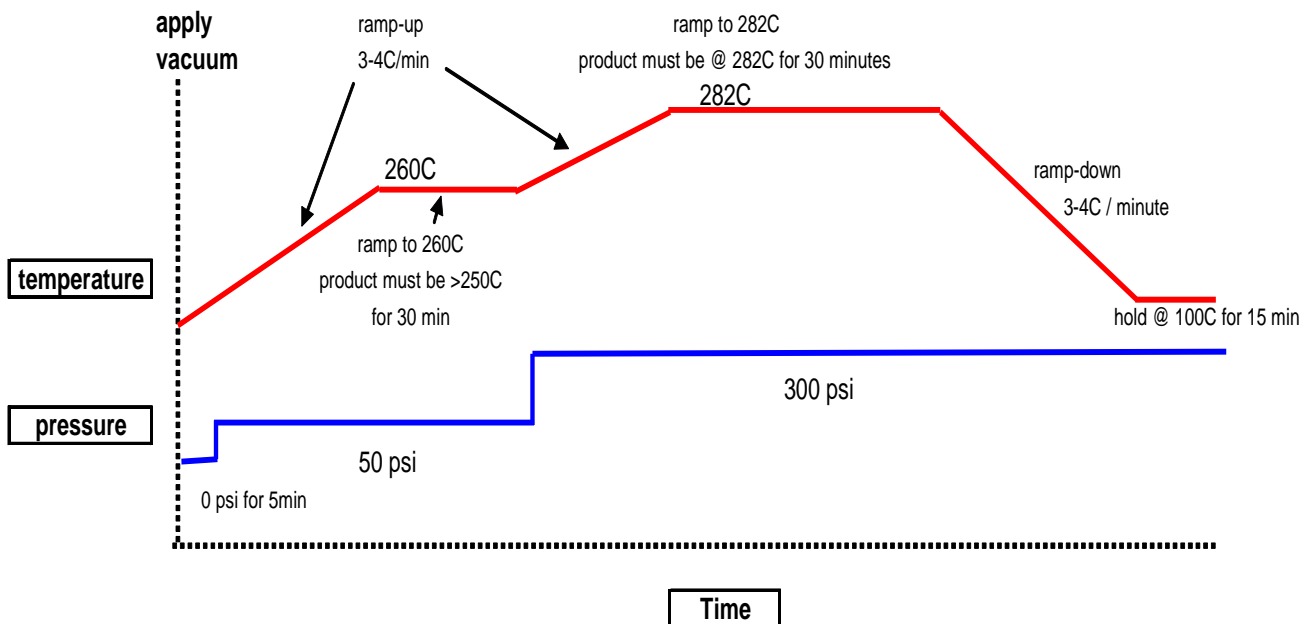


Figure 12. High temperature LCP lamination cycle

The drilling operation is also important and has similar concerns as drilling PTFE substrate. The main concern is to minimize the risk of smearing the substrate, which

means minimizing the heat generation during the drilling process. Parameters for drilling LCP are shown in figure 13.

Chip Load	0.001" to 0.002"/rev.
Spindle Speed	200 to 500 SFM
Retract Rate	200 to 600 IPM
Entry Material	0.007" Aluminum
Exit Material	Phenolic

Figure 13. Drilling conditions for LCP multilayers

When drilling small holes or high aspect ratio a peck drilling procedure may be needed. The maximum peck depth should not exceed 0.015". The drill tool should be high quality carbide and only use new tools.

The drilled hole-wall preparation for PTH can use either a chemical process or a plasma process. The chemical process uses a high concentration KOH. The plasma process is recommended and the parameters for this process are shown in figure 14.

Segment	Gas Type, %				Vacuum, mTorr	Temperature, C	Time, min.
	CF <sub>4</sub>	O <sub>2</sub>	N <sub>2</sub>	H <sub>2</sub>			
1	0	80	20	0	250	70	45
2	10	80	10	0	240	105	25
3	0	0	90	10	250	105	60

Figure 14. Plasma process for LCP substrates

There are many PCB applications where combinations of different circuit materials are used. Some applications will have high frequency circuit materials used on the PCB layers that are critical to electrical performance, while the other layers may use FR4 materials.

A common hybrid circuit will use one layer of a non-PTFE ceramic filled substrate for layers 1 and 2, which will make up a high frequency microstrip transmission line. The other layers of the PCB will be more traditional PCB materials such as FR4 and are not electrically critical. With layer 1 being the signal and layer 2 the ground plane, the bonding materials below layer 2 can be FR4 prepreg. These hybrids can typically be manufactured with good yields assuming some caution is taken in a few processes. One area of concern would be the unbalance of material types and a possible warp issue. The most effective procedure to minimize the warp issue of the mixed materials is during the lamination cycle, specifically at the end of the cycle and after the prepreg is fully cured – minimize the pressure to 50 psi and hold for 30 minutes. This low- pressure cycle is held while still at the cure temperature.

Another common hybrid circuit will use a combination of PTFE circuit materials and FR4. The critical electrical layers will use the PTFE substrate and the other layers would be the FR4. More often a ceramic filled PTFE substrate is used, because it will have a

closer match to the FR4 thermal / mechanical properties and has a simpler PCB process. The PTFE substrate will typically not cause a warp issue because the PTFE is very soft compared to the FR4. During the lamination cycle the FR4 substrates will expand / shrink due to the temperature excursions, and the PTFE will be so soft that it will follow the FR4 movement. The drilling must be tailored to be optimal for the PTFE and the preparation for PTH will have several stages. The first stage is to de-smear and treat the FR4 material as necessary for the PTH preparation. The next stage will be to treat the PTFE for the PTH process. If a wet PTH preparation process is used for either the FR4 or the ceramic filled PTFE, then a bake at 121°C (250°F) for 1 to 2 hours is necessary just prior to the copper plating process.

A more exotic hybrid combination that has potential to be extremely good for high frequency applications and have mechanical flexibility is a special Rigid-Flex construction. This circuit would use the LCP materials for the flexible portion and would use the non-PTFE ceramic substrates for the rigid portion. This combination would have several advantages. The transition from the rigid board areas to the flexible areas will not have connectors and the connection is built into the circuit. The lack of connectors means the cost for the connectors, assembly, and reliability issues of connectors goes away. Also, if the design accounts for the transition from the rigid material to the flexible materials correctly there can be no impedance difference and that means a clean signal transition. For this type of circuit the drill parameters will need to use the LCP parameters. The plated through hole preparation will be a several stage process as previously described. The last stage of the preparation process will be for the LCP materials.

In summary, PTFE substrates are typically more difficult for circuit fabrication and will have superior electrical performance. The best material for electrical performance is the nearly pure PTFE substrates. These types of materials have been used for the most demanding electrical applications and have very specific fabrication guidelines. Guidelines for this type of material can be found at <http://www.rogerscorp.com>. Adding ceramic filler to the PTFE will lower the CTE, which is good for multilayer circuits and good PTH reliability. This addition also makes the material friendlier to PCB fabrication, however slightly degrades the electrical performance.

The non-PTFE materials are typically the most friendly to the PCB fabrication process and can have good electrical properties. There are many types of prepreg that can be used with this type of material and most of them have very different processing guidelines. Lastly, the LCP materials offer a multitude of benefits to many applications. However, the PCB fabrication process requires special equipment and must be well controlled.

References:

[1] John Coonrod, “Bending and Forming High Frequency Printed Circuits”, IPC Printed Circuits Expo<sup>®</sup>, APEX<sup>®</sup> and the Designers Summit, 2007.

[2] Thompson, Kirby, Papapolymerou, Tentzeris, “W-Band Characterization of Finite Ground Coplanar Transmission Line on Liquid Crystal (LCP) Substrates”, *IEEE Polytronic Conference 2003*.

Much of the fabrication information given can be found at:

<http://www.rogerscorp.com/acm/index.aspx>

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