Void Reduction during Low Pressure Lamination of Electronic Assemblies

David C. Timpe Jr.* and Andy Cloud
Arlon – Silicone Technologies Division
1100 Governor Lea Road, Bear, DE 19701

Abstract

Void content at the interface of the bonding adhesive and rigid substrate of an electronic assembly can affect critical performance metrics such as thermal transfer, bond strength, and stress decoupling which can ultimately lead to poor device reliability. In this paper, the contribution of substrate size and lamination method on void content is investigated. It is shown that void content increases with increasing air escape path length. Since the voids are pockets of air entrapped during lamination, the best way to minimize void formation at low lamination pressures is to assemble the laminate in the absence of air, i.e., under vacuum. Differential vacuum pressure lamination (DVPL) is an alternative to the standard vacuum bag process widely utilized today for lamination of populated electronic assemblies. It is shown that the DVPL process dramatically reduces void content at the adhesive interface while maintaining comparable rates of throughput. Data are also provided linking this reduction in void content to improvement in critical performance metrics, demonstrating that using the DVPL process will achieve increased component reliability. The experiments were conducted with a commonly used silicone-based, heat cured, thermal interface adhesive, Arlon's G2p Thermabond®.

Key words: void reduction, lamination, thermal interface material, reliability

Introduction

Electronic assemblies, consisting of a populated printed circuit board (PCB) bonded to a heat sink with a thermal interface material (TIM) adhesive, are used in electronic applications ranging from automobiles to satellites. The operation of the surface mounted electronic components of the PCB depends in part on the ability of the assembly to dissipate thermal energy through the adhesive to the heat sink. Void content at the interface of the adhesive affects not only thermal transfer but also bond strength and stress decoupling. Interfacial voids are of particular concern when laminating populated PCBs because the surface mounted electronic components are delicate and create surface topography that precludes the use of a hydraulic platen press and necessitates the use of a conformal, low pressure lamination process.

Void content at the adhesive interface can affect critical performance metrics. It has been shown that voids in the thermal interface layer increase thermal resistance and hinder heat flow from the PCB to the heat sink [1, 2]. This can result in temperature fluctuations and reduced life expectancy [1]. Voids have also been linked to reduced adhesive strength and reliability [3]. Inferior PCB to heat sink adhesive attachment strength can lead to blisters or delamination during in-service thermal cycling.

Populated PCBs must be laminated with a conformal, low pressure process because of the surface topography and delicacy of the surface mounted electronic components. Two applicable processes are the vacuum bag process and the differential vacuum pressure laminator (DVPL) process. Both processes use an elastomeric sheet to conform to the topography and a vacuum pump to create a maximum lamination pressure of one atmosphere. The processes differ during the application of the PCB to the adhesive coated heat sink. This step is performed at atmospheric pressure in the vacuum bag process and under vacuum in the DVPL process.

This research investigates the effect of lamination method and laminate size on voiding at the adhesive/PCB interface. Glass plates laminated with a silicone rubber TIM adhesive are digitally imaged and void area is calculated through a threshold limit. Additionally, the effect of interfacial voids on thermal resistance and adhesive shear strength is investigated.

Problem Definition

Lamination of an electronic assembly in the vacuum bag process can result in voids at the interface of the adhesive and PCB. Voids can increase thermal resistance, decrease adhesive strength and affect stress decoupling which can result in poor device reliability [1, 2, 3]. Populated PCBs are typically laminated to a metallic heat sink using a vacuum bag process consisting of three steps:

1) Application of the adhesive to the heat sink;
2) Application of the populated PCB to the adhesive coated heat sink;
3) Curing of the adhesive.

The adhesive is initially applied to the heat sink using a nip roller lamination method. The use of a nip roller at this stage is made possible by the flexibility of the adhesive. The nip roller facilitates the removal of air at the interface of the adhesive and heat sink producing an interface that is free of trapped air (see Figure 1).

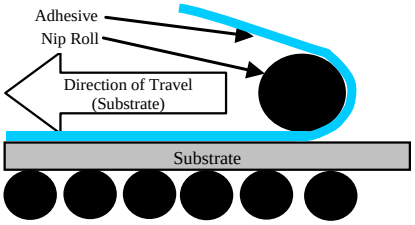


Figure 1 – Diagram of a simple nip rolling procedure for applying the adhesive to the first substrate.

The populated PCB is laminated to the adhesive at atmospheric pressure by aligning it and gently mating it to the adhesive. This step may be performed by hand or by use of a registration system. Air is likely to be trapped between the PCB and adhesive resulting in a void after the cure cycle. It is not possible to flex the rigid PCB during lamination because of the PCB architecture and surface mounted components so a nip roll cannot be used to facilitate air removal.

The adhesive is cured in a vacuum bag under atmospheric pressure or less and a temperature appropriate for the adhesive, the PCB, and the electronic components. At this low pressure the air entrapped during the application of the PCB to the adhesive coated heat sink remains at the interface becoming an interfacial void in the final assembly.

The vacuum bag process typically used for lamination of populated PCBs can create voids at the interface of the adhesive and PCB. These voids are the result of air entrapped during lamination of the PCB to the adhesive. Voids are less likely at the interface of the adhesive and heat sink because the nip rolling process is effective at removing air at this interface. The cure cycle is not able to remove the trapped air because of the low lamination pressure required for a populated PCB.

Method of Solution

Voids at the interface of the populated PCB and adhesive can be reduced during low pressure lamination if air is removed during lay-up of the populated PCB and adhesive. A differential vacuum pressure laminator (DVPL) is used to laminate a populated PCB to an adhesive coated heat sink under vacuum pressure. A registration system, internal to the laminator, maintains spacing between the PCB and adhesive until vacuum pressure has been reached.

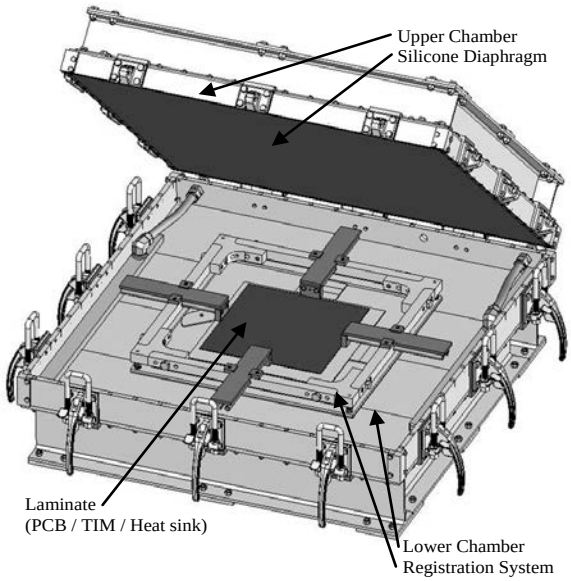


Figure 2 – Computer model of the differential vacuum pressure laminator.

A DVPL is used for conformal, low pressure lamination of a populated PCB to a heat sink with a TIM adhesive. The DVPL utilized in this research was developed through a partnership with the Mechanical Engineering Department at the University of Delaware. The DVPL is an aluminum enclosure separated into an upper and lower chamber by a 0.060 in. thick silicone rubber diaphragm. The silicone rubber diaphragm is the same type that is used for reusable vacuum bags. It enables differential pressure between the chambers and applies pressure to the populated PCB. Silicone rubber is ideal for this application because of its low modulus, high elongation, and for its resistance to

compression and tension set. Heat is supplied by two wire wound flexible silicone rubber heaters with embedded thermocouples capable of supplying 3200 watts (O&M Heaters, Japan). The heaters are controlled by a Precision Digital PD 554 ramp and soak controller. Vacuum is supplied by a single standard laboratory style vacuum pump capable of supplying an absolute pressure of $< 1x10^{-3}$ atmospheres. The lamination cycle is controlled by an Omron CPM1A programmable logic controller (PLC).

A registration system maintains spacing between the PCB and adhesive coated heat sink until vacuum pressure has been reached. This allows the PCB and adhesive to be laminated without trapping air at the interface. The PCB is held along its edges by four spring-loaded clamps that are held by a square frame. The frame is held aloft with a spring and pin at each corner. The silicone rubber diaphragm compresses the frame springs bringing the PCB into contact with the adhesive during lamination.

The combination of the DVPL and registration system allows the amount of air at the interface of the adhesive and PCB to be reduced, or possibly or possibly be eliminated depending on the vacuum pump, before contact is made. This reduces the amount of air that is trapped between the adhesive and PCB that results in interfacial voids after the cure cycle.

Experiment

The effect of lamination method and laminate size on void content at the PCB/adhesive interface was investigated through a 2x2 full factorial design of experiments (DOE) (see Table 1). The DOE produced four experimental runs that were performed by two operators with two lots of adhesive to introduce natural variability. The adhesive is a 0.008 in. thick silicone rubber TIM adhesive (Arlon, Bear Delaware, G2p Thermabond® P/N: 99990A008). The experiment was performed on 0.125 in. thick, double strength, float glass plate. Glass plates were chosen because they are rigid and planar and the PCB/adhesive voids can be viewed and imaged fairly easily.

The glass substrates were prepared for lamination by cleaning in a mild solution of soap and water followed by wiping with isopropyl alcohol and a lint free cloth to remove contamination that may interfere with adhesion. The adhesive was applied to half of the cleaned glass plates using a nip roll process (see Figure 1). The nip roll process successfully applied the adhesive without entrapping air.

Table 1 – Design of the 2x2 Full Factorial DOE.

2x2 DOE	Factor 1	Factor 2
	Laminate size	Lamination Method
Level – Low	4 in. x 4 in.	Vacuum Bag
Level – High	6 in. x 8 in.	DVPL

Laminates cured in the vacuum bag process were prepared by aligning and lightly placing a clean glass plate onto the original adhesive coated plate by hand. The laminate was immediately transferred to a silicone rubber vacuum bag, breather cloth was laid over the laminate and vacuum was drawn to an absolute pressure of 0.1 atmospheres. The vacuum bag was placed in a hot air convection oven at 121°C for 60 minutes. The vacuum bag assembly required 45 minutes to reach temperature to which an additional 15 minutes was added to fully cure the adhesive. At the end of the 60 minute cycle the laminate was removed from the vacuum bag assembly and allowed to cool to room temperature.

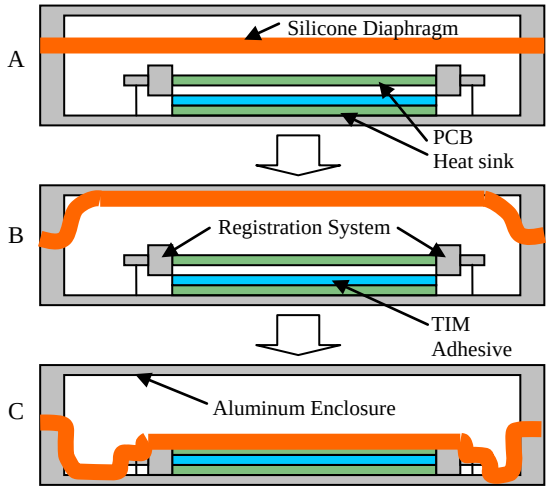


Figure 3 – Schematic of the DVPL lamination process. (A) Atmospheric pressure in both chamber of DVPL with the PCB separated from the adhesive by the registration system. (B) Vacuum drawn in top chamber of DVPL. (C) Vacuum drawn in bottom chamber and top chamber vented to atmosphere. Silicone diaphragm has descended, mated the PCB to the adhesive, and is applying pressure to the assembly.

Laminates cured in the DVPL process were prepared by securing a clean glass plate in the

registration system positioned above the original adhesive coated plate. The DVPL was sealed and a cycle initiated on the PLC. The cycle consisted of drawing both chambers to vacuum (0.1 atmosphere) to reduce the amount of air at the adhesive interface before laminating. The top chamber was then vented to atmosphere to compress the registration system and perform the lamination (see Figure 3 – Glass plates were used as the PCB and Heat Sink). The PD 554 controller was activated and the programmed cycle run (see Figure 4). At the completion of the cycle the bottom chamber was vented to atmosphere and the laminate was removed and cooled to room temperature.

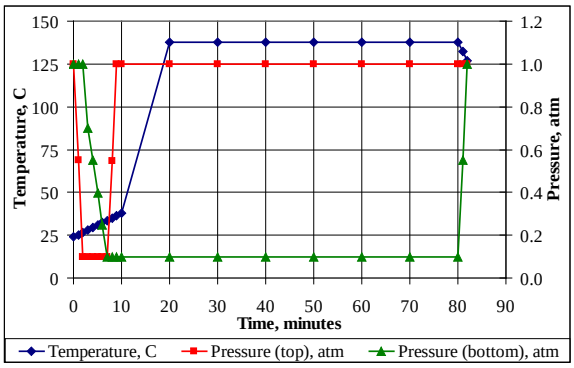


Figure 4 – Temperature and pressure cycle of the differential vacuum pressure laminator.

Twelve laminates for each run for a total of 48 laminates were prepared and imaged using a digital scanner. Void area was calculated as a ratio of the void area to total area of each laminate based on a threshold value determined for each scanned image. This approach worked well due to the difference in refractive index of where the adhesive is and is not bonded to the glass.

Results and Discussion

The 2x2 full factorial designed experiment was analyzed by two-way analysis of variance (ANOVA) (see Table 2a, 2b, & Figure 5). The lamination process has a statistically significant effect on void ratio. The average void ratio for both laminate sizes produced by the vacuum bag process is 0.635 and the average void ratio for both laminate sizes produced by the DVPL process is 0.149. The DVPL process performed the lamination at 0.1 atmospheres which reduced the amount of air trapped at the interface resulting in 77% less voiding in the final laminate. Reducing the pressure further is expected to yield an even greater reduction in void ratio. A lower void ratio is desirable since it means a higher percentage of the area is well bonded. The laminate size also produced a statistically significant effect on void ratio. The average void ratio for both lamination processes of the 4 in. x 4 in. laminate is 0.354 and the average void ratio for both lamination processes of the 6 in. x 8 in. laminate is 0.431. As expected, the void ratio increased as laminate size increased due to a longer air escape path length. The data are normally distributed and the variances are similar.

Table 2a – Two-way ANOVA. Effect of lamination method factor on void ratio.

	Lamination Method
Average at Low Setting Vacuum bag process	0.635
Average at High Setting DVPL Process	0.149
Δ	-0.486
Δ/2	-0.243
|Δ/2|	0.243
Mean Square Between	2.835
Fo	1799.258
Fc	18.304
Fr	98.300
Confidence Level	99.99%

Table 2b – Two-way ANOVA. Effect of laminate size factor on void ratio.

	Laminate Size
Average at Low Setting 4 in. x 4 in.	0.354
Average at High Setting 6 in. x 8 in.	0.431
Δ	0.078
Δ/2	0.039
|Δ/2|	0.039
Mean Square Between	0.072
Fo	45.738
Fc	18.304
Fr	2.499
Confidence Level	99.99%

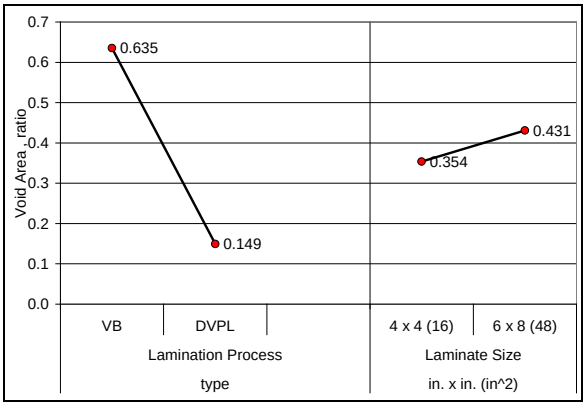


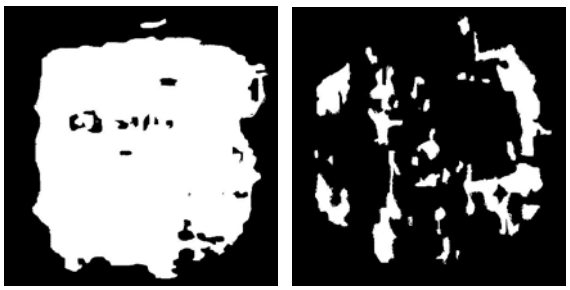
Figure 5 – Factor level average void ratio.

The effect of laminate size on void ratio was further investigated by one-way ANOVA (see Table

3) for each lamination process. The laminate size has a statistically significant affect on void ratio in the vacuum bag process. The vacuum bag process produces an average void ratio of 0.567 on a 4 in. x 4 in. laminate and an average void ratio of 0.704 on a 6 in. x 8 in. laminate (see Figures 6A & 7A). The laminate size factor does not have a statistically significant affect on void ratio in the DVPL process. The DVPL process produces an average void ratio of 0.140 on a 4 in. x 4 in. laminate and an average void ratio of 0.158 on a 6 in. x 8 in. laminate (see Figures 6B & 7B). The void ratios produced by the DVPL process on both laminate sizes are considered part of the same larger population based on the confidence level of only 69%. The effect of laminate size on void ratio is eliminated by reducing the amount of air at the interface during lamination. This is achieved by laminating under vacuum pressure in the DVPL process.

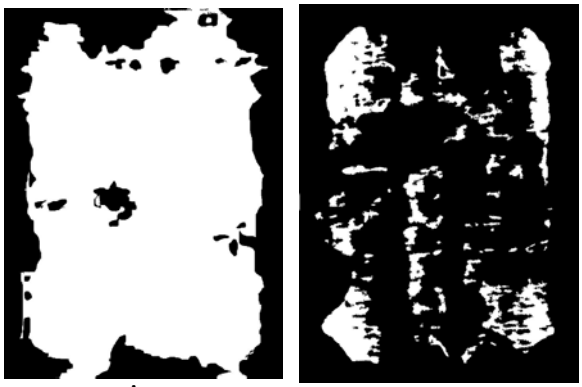
Table 3 – One-way ANOVA. Effect of laminate size on void ratio in vacuum bag process and DVPL process.

	Vacuum Bag Process	DVPL Process
Factor Average when Laminate Size = 4 x 4 (16), in (in^2)	0.567	0.140
Factor Average when Laminate Size = 6 x 8 (48), in (in^2)	0.704	0.158
Δ	0.137	0.018
Δ/2	0.068	0.009
|Δ/2|	0.068	0.009
Mean Square Between	0.112	0.002
Fo	85.923	1.065
Fc	22.431	1.064
Fr	3.831	1.001
Confidence Level	99.99%	68.65%



A. B.

Figure 6 – Typical scan of a 4 in. x 4 in. laminate produced in (A) the vacuum bag process with 0.548 void ratio, (B) in the DVPL process with 0.140 void ratio (right). White area indicates void.



A. B.

Figure 7 – Scan of a 6 in. x 8 in. laminate produced in the (A) vacuum bag process with 0.695 void ratio, (B) in the DVPL process with 0.150 void ratio. White area indicates void.

The effect of operator and adhesive lot on void ratio was investigated for each run of the 2x2 DOE by one-way ANOVA. Neither the operator factor nor the material lot factor significantly affects the void ratio based on a confidence level of 95%.

The effect of void ratio on thermal resistance was investigated by preparing 6 in. x 8 in. - aluminum / adhesive TIM / aluminum laminates in both the vacuum bag and DVPL processes. Thermal resistance was measured by modified ASTM D 5470 [4] on 1.25 in. diameter disks machined from laminates prepared in both lamination processes. ASTM D 5470 was modified to use a reduced stack pressure of 5 lbf. and 50 lbf. to reduce the likelihood of the adhesive TIM interface and the aluminum interface coalescing in voided areas. The DVPL process produces a laminate thermal resistance 9% and 4% lower than the vacuum bag process at a stack pressure of 5 lbf. and 50 lbf, respectively. One-way ANOVA returns confidence levels of 99% and 94% at stack pressures of 5 lbf. and 50 lbf, respectively. The change in thermal resistance at different stack pressures indicates the adhesive TIM and aluminum interfaces are coalescing in voided areas. The difference in thermal resistance produced by the two processes in an actual application is expected to exceed 9% because the void areas are not coalesced by an external force.

The effect of void ratio on adhesive attachment strength was investigated by preparing 6 in. x 8 in. - aluminum / adhesive TIM / epoxy laminates in both the vacuum bag and DVPL process. Shear strength was measured by ASTM D 1002 [5] on single-joint lap shear coupon machined from laminates prepared with both lamination processes. The average shear strength obtained in the vacuum

bag process is 222 PSI and the average shear strength obtained in the DVPL process is 925 PSI. One-way ANOVA returns a confidence level of 99%, indicating that the DVPL process produces a statistically significant higher TIM shear strength than the vacuum bag process. The increased shear strength produced with the DVPL process is the result of reduced voiding at the adhesive interface.

Conclusion

The DVPL process is superior to the vacuum bag process for lamination of populated electronic assemblies. Lamination quality via the DVPL process is independent of laminate size unlike the vacuum bag process, which produces a significantly higher void ratio as the laminate size increases. A 77% reduction in void ratio is realized across laminate sizes ranging from 16 in^2 – 48 in^2 with the DVPL process. The reduction in void ratio results in a 317% increase in adhesive shear strength and a reduction in laminate thermal resistance of at least 9%. Improvement in these critical performance metrics is expected to translate into greater electronic device and component reliability.

Acknowledgment

The authors would like to thank the University of Delaware Senior Design Team; Doug Brunner, Adam Fauer, Claire Jones, and Michael Klein, their Advisor Dr. Jim Glancey and Geno Amalfitano, Sr. R&D Technician, Arlon, for their devoted assistance.

References

[1] Dimosthenis C. Katsis and Jacobus Daniel van Wyk, “Void-Induced Thermal Impedance in Power Semiconductor Modules: Some Transient Temperature Effects”, IEEE Transactions on Industry Applications, Vol. 39, No. 5, pp. 1239-1246, September/October, 2003.

[2] Arun Gowda, David Esler and Sandeep Tonapi, “Voids in Thermal Interface Material Layers and Their Effects on Thermal Properties”, 2004 Electronics Packaging Technology Conference (EPTC), pp. 41-46, 2004.

[3] Muffadel Mukadam, Jeff Schake, Peter Borgesen and Krishnaswami Srihari, “Effects of Assembly Process Variables on Voiding at a Thermal Interface”, Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM 2004, The Ninth Intersociety Conference, Vol. 1, pp. 58-62, 2004.

[4] ASTM D 5470-01 “Standard Test Method for Thermal Transmission Properties of Thin Thermally Conductive Solid Electrical Insulation Materials”, December, 2001.

[5] ASTM D 1002-99 “Standard Test Method for Apparent Shear Strength of Single-Lap-Joint Adhesively Bonded Metal Specimens by Tension Loading (Metal-to-Metal)”, December, 1999