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COVER STORY

Creating Wireless SiP Solutions

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IC packaging has become a critical bottleneck to achieving reductions in the size of wireless products. The deployment of new broadband wireless standards, based on multiple-input-multiple-output (MIMO) technology, means that mobile phones, laptops, and mobile Internet devices will require increasingly complex front-end circuitry. With up to 10 power amplifiers (PAs) and associated low-loss RF filters, couplers, and matching circuits, circuit board area required for future front-ends will surpass that required for digital processor and memory functions implemented in CMOS. CMOS SoC solutions have only proven to be acceptable in low-power applications, thus RF front-ends are still composed of heterogeneous RFIC technologies along with discrete passive components. As a result, RF system-in-package (SiP) technology is an enabler of the next-generation of wireless products.

THE SHORT STORY

While CMOS SoC works well in low power applications, it doesn't meet requirements for future wireless products. RF system-in-package (SiP) is one option, but existing solutions are costly, or don't reach the necessary level of integration. A thin-film multilayer process for embedding passives is another option.

Existing solutions based on ceramic packages or silicon passive components are either expensive, or not capable of reaching the level of integration needed. However, a patented, thin-film, multi-layer process to implement RF SiP substrates — multi-layer organic (MLO) packaging — provides a vehicle to embed critical RF passive components into a substrate underneath the RFICs while maintaining low insertion loss and high isolation (Figure 1).

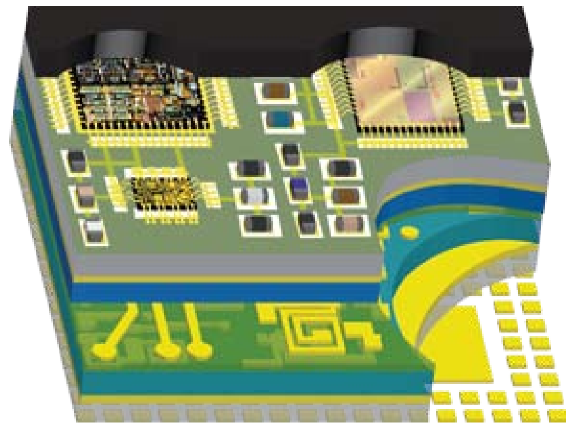

FIGURE 1. MLO SiP

MLO combines advanced RF circuit materials based on liquid crystalline polymers (LCP) and ceramic-filled polytetrafluorethylene (PTFE) composites, coupled with novel processing and circuit topologies. To maximize integration capability for critical high-frequency components, these materials are designed to have low loss at high frequencies, stable dielectric constant, good laser microvia capability, low moisture absorption, and good thermal stability contributing to favorable overall package reliability. More than just a packaging technology, MLO represents a fundamental change in the method of designing compact RF systems.

MLO History

MLO is an outgrowth and continuation of packaging research funded by the National Science Foundation at the Georgia Tech Microelectronics Packaging Research Center (PRC). Although there are multiple packaging alternatives for 3D SiP applications, the most promising approaches focus on solutions where thin organic dielectric materials and embedded components are inherent. This technology has been applied to develop a variety of RF products including stand-alone passive components, highly integrated RF front-end-modules (FEMs), and embedded modules containing the complete wireless chipset and front end.

Other alternatives for RF multi-chip packages, such as low temperature co-fired ceramic (LTCC) and conventional laminate substrates, are limited with regard to increased complexity and shrinking geometries. LTCC is a mature packaging technology, but is costly and suffers from temperature-related failures due to CTE mismatch with common PCB materials. It is also difficult to inte-

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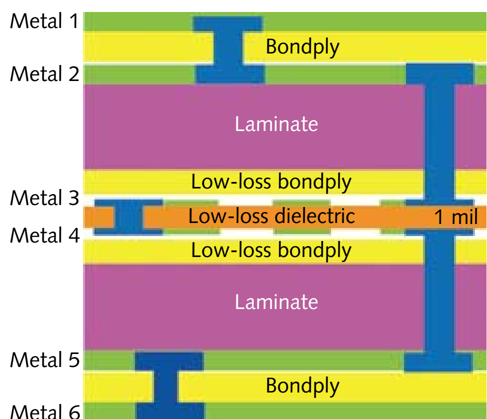

FIGURE 2. MLO stack-up.

grate RF, digital, and mixed-signal technologies in LTCC due to package size limitations. An organic laminate system capable of high Q embedded passive components provides advantages over ceramic and IC processes, such as short cycle time, low cost, and wide availability of HDI organic laminate processing capacity. Equal or better performance is obtained with only six metal layers of MLO when compared with the same functionality obtained with 12-20 layers of LTCC. While there have been other attempts to embed passive components into organic laminates, most of these have addressed non-RF passives such as resistors and decoupling capacitors.

MLO Substrate Construction

An MLO substrate consists of one or more RF dielectric layers embedded between layers of other laminates to provide routing, shielding, and bonding areas for SMT and RFIC die placement. Figure 2 shows a typical "stackup". Silica-filled hydrocarbon bondplys and laminates are used for the outer layers to provide rigidity, low moisture absorption, and low z-axis CTE to help ensure reliability. Inner dielectric layers must have low loss at the operating frequency, and should be thin to enable higher capacitance densities and minimize total package height. The development of low-loss, dimensionally stable laminates based on LCP as thin as 25 µm allowed initial capacitance and Q requirements to be met. The LCP dielectric is unfilled with a low Er and tan δ that is useful for a variety of RF and high-speed applications. High dielectric constant is preferred so designers achieve higher capacitance densities. To meet this need, a 25 µm PTFE composite has been developed using advanced filler materials to increase Er without significantly increasing loss. This gives the designer options for either low or high dielectric constant in the inner layer, depending on each application. Standard multi-layer and/or sequential lamination processing can be used to produce completed package structures. The finished MLO substrate exhibits excellent RF performance as a result of the low-loss dielectric materials and the use of shielding layers above and below these low loss dielectric layers (Figure 3). Properties of dielectric materials used in the MLO stack-up are summarized in Table 1.

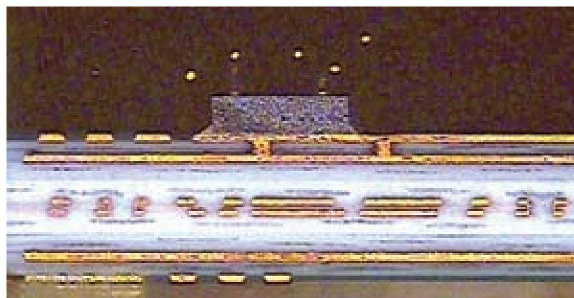
FIGURE 3. MLO module cross section.

Process Control

The ability to monitor process parameters and predict their impact on device yield is essential to put MLO-based products into volume production. Although fabricated from laminate materials, a MLO panel is treated like an RF semiconductor wafer from the perspective of process control and testing. The most critical parameters for controlling embedded component tolerances are the core layer thickness, layer-layer registration, and line width/spacing on the dielectric layers. The derivation of these parameters is a complex process involving tradeoffs between fabricator capabilities and RF design parameters. Since tighter control over these critical parameters inevitably leads to higher costs, care has been taken to develop process-tolerant component designs that produce high yields without requiring significant investment in fabrication technology.

Design for manufacturability (DFM) was an important element in MLO development. Tools that facilitate the task of designing high-yield products were developed. As in semiconductor fabrication, process control monitor (PCM) structures allow rapid measurement of key process parameters post fabrication. Along with automated optical inspection (AOI) data, PCM measurements are used to refine device models and to provide feedback to laminate fabricators. Novel PCM structures yield measurements that are highly correlated with material and process parameters by using simple DC and low-frequency probes.

RF Component Structures

To take full advantage of the embedded device capabilities of MLO, product designers need the ability to implement the common components used in RF systems rapidly, such as matching networks, filters, baluns, couplers, and diplexers. These components can be implemented in a wide range of circuit topologies but must be ultimately transformed into lumped element structures consisting of embedded inductors, capacitors, and transmission lines. These structures are etched into the copper-clad dielectric layer along with internal shielding layers, LGA pads and die-attach structures (Figure 4).

Property	Inner layer, low K	Inner layer, high K	Outer layers
Er @10 GHz	2.9	7.6	3.3-3.6
tan δ @ 10 GHz	0.0025	0.0025	.004
Water absorption	0.04%	<0.2%	0.1%
x/y CTE (ppm/C)	17	30-50t	15-17
z-axis CTE (ppm/C)	150	45	50
Thermal conductivity (W/m/K)	0.2	0.5	0.6
Thickness (µm)	25	25	75-100

TABLE 1. Key dielectric layer properties

Because small form-factor packages

require high component densities, these structures must be designed to provide the desired level of performance in the presence of coupling and ground conductor proximity. The Q-factor of embedded components is also critical to ensure low-loss. Particularly in inductor design, structures must be modeled and tested to insure that desired Q-factors can be maintained. For this reason, designers must be provided with 'known good structures' for common functions at the various frequency bands used in wireless systems. Inductor Qs of over 150 have been achieved at 3 GHz with MLO. This compares with Qs of 20-50 with silicon-integrated passive devices or conventional laminates.

As a result of its multiyear efforts in developing MLO, an extensive library of RF components exists for product designers to re-use in new designs. For example, a 2.6 GHz balanced bandpass filter was initially synthesized using standard RF design tools and then implemented in a two-layer spiral structure. The filter achieves an in-band insertion loss of 1.8 dB, and out-of-band rejection from 4.1 to 4.5 GHz of 40 dB and 45 dB below 2 GHz.

Reliability

Any novel IC packaging technology must meet the stringent reliability requirements of the consumer electronics industry. Due to the inherent low moisture absorption of the materials used in MLO, modules using this substrate technology are expected to be highly reliable. Front-end modules containing both GaAs and SiGe die, assembled with standard wire-bond assembly techniques, have been subjected to JEDEC reliability stress testing, under an LTPD 5% sampling plan (0 rejects allowed per 45 samples, per lot) with no failures or performance degradation. Modules passed MSL 3/260 preconditioning (J-STD-020C), unbiased HAST (JESD22-A118, condition A), 500 hours HTOL (JESD22-A108C), 500 temperature cycles (JESD22-A104C, condition G, soak mode 4), and biased HAST (JESD22-A110, condition A).

Conclusion

A reliable, high-performance organic package with embedded passive components has long been sought by the semiconductor industry. MLO has shown that such a goal is obtainable, and that organic packages are capable of challenging conventional multi-layer ceramic technology for the next generation of wireless SiP products. **AP**

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