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Navigating Multilayer Microwave PCB Tradeoffs

There are numerous ways to assemble multilayer microwave printed circuits, depending on whether cost or performance is important, and when factors such as ease of fabrication and reliability are critical.

Microwave printed-circuit-board (PCB) transmission-line technologies are fairly well known—including microstrip, stripline, and coplanar-waveguide (CPW) technologies—and commonly used on PCBs. Because of size and volume constraints, however, high-frequency circuit designers are increasingly working with multilayer PCBs, which are formed from multiple copper-clad substrates and bonding layers. Achieving successful multilayer PCBs requires some knowledge of how these circuits are fabricated, as well as an understanding of the special requirements for multilayer PCBs compared to single-layer circuits.

To better understand the microwave multilayer circuit fabrication process, it may help to use a stripline transmission line as an example circuit. Stripline is commonly used at microwave frequencies for both passive and active circuit designs. It consists of two outer metal layers that act as ground planes and a single inner layer that acts as the signal or conductive layer. The metal layers are separated by dielectric substrate material. For PCBs, the layer-naming convention is based on a count of the conductive layers and, in a stripline circuit with one signal or conductive layer, there are technically three conductive layers when the two ground layers are included.

In this simple example, the stripline circuit is fabricated with the aid of bonding material called a prepreg, surrounding the copper-clad laminate that holds the signal layer. The prepreg layers are essentially uncured dielectric substrates that are used to bond the copper-clad laminate to another raw copper foil layer to form the three copper planes—the two ground planes and the signal plane—of the stripline circuit.

In this PCB construction, the prepreg acts like a glue layer, bonding multiple layers together. In order to form a strong bond, the prepreg must go through a lamination or curing process in which the layers to be bonded are maintained under pressure and at an elevated temperature; the type of prepreg and its material properties will determine the curing time and temperature for this process. During the early stages of the cure cycle, the prepreg will assume a gel state and will “flow” around the features of the other layers to be bonded. This flow-
ing of the prepreg enables the material to fill in spaces and pocket areas between copper circuits and any irregularities in the laminate substrate surface, ensuring that the prepreg’s dielectric material has filled any holes and created a more predictable electrical structure with no air gaps (which exhibit a different dielectric constant).

Figure 1 shows a block diagram of the various stages of the stripline PCB fabrication process. The process starts with a copper-clad laminate, upon which one of its copper layers is selectively etched to form the circuit’s signal layer; the other copper layer will form one of the stripline circuit’s ground planes. Layers of prepreg material are then added to the laminate, with a copper foil layer on top to form the second stripline ground plane. These multiple layers are then treated to a lamination process where the prepreg is cured under pressure and temperature to form a strong bond among the different layers.

Figure 1 does not show an important part of the stripline circuit: how electrical connections are made from the outside world to the signal layer. This is achieved by drilling holes through the PCB, in areas aligned to the circuit pattern. These drilled holes are then coated with copper to create electrical paths which are called plated through holes (PTHs). For consistent stripline circuit performance, it is critical to maintain both the top and bottom ground planes at the same electrical potential, so the PTHs are essential for making the electrical connections between the top and bottom ground planes. For this type of stripline circuit, an RF/microwave connector is typically mounted on the top of the circuit assembly, and the connector’s signal launch uses a PTH for an electrical path to the inner conductor or signal layer. Figure 2 shows a cross-sectional photo of an actual stripline circuit and its three copper layers.

Most multilayer microwave PCBs can be assembled in a number of different ways, and each approach has its own benefits and limitations. For example, in addition to the method described earlier, the example stripline circuit could be fabricated by using two copper-clad laminates and less prepreg material. With these starting materials, the first part of the fabrication process would be the same, with one of the copper layers of one of the laminates etched to form the circuit’s signal or conductive layer. For the lamination process in this second case, a thin layer of prepreg would be added and then the second copper-clad laminate, except that this second laminate would have all of the copper removed from one side. This side is where the prepreg will be used to bond to the etched signal layer. Figure 3 shows how the example stripline circuit is formed with this fabrication approach; the PTHs connect the top and bottom ground planes which, in this case, are copper layers on what initially were separate laminates.

If both of these fabrication approaches result in a stripline circuit, why use one method instead of the other? The first method, shown in Fig. 1, is more cost-effective, since prepreg materials are typically lower in cost than copper-clad laminates. That first method only used one copper-clad laminate, several prepreg layers, and a copper foil layer compared to the second approach, which employed two copper-clad laminate layers (albeit with less prepreg material). The cost of the second laminate layer outweighs the cost of the other additional materials in the first method.

What must also be considered is that the properties of a prepreg often differ

<table>
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<tr>
<th>Comparing common bonding materials.</th>
<th>Dielectric constant</th>
<th>Dissipation factor</th>
<th>Ease of fabrication</th>
<th>Robust soldering</th>
<th>Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bonding material</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR-4 (industry standard, baseline)</td>
<td>4.5</td>
<td>0.0180</td>
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<td>FEP</td>
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<td>0.0010</td>
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<td>0</td>
<td>0</td>
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<tr>
<td>Chloolfluoro-copolymer</td>
<td>2.3</td>
<td>0.0030</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Ceramic-filled hydrocarbon prepreg</td>
<td>3.9</td>
<td>0.0040</td>
<td>0</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>LCP</td>
<td>2.9</td>
<td>0.0025</td>
<td>–</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: For relative ratings, 0 means on par, – means less than average, and + means more than average.
from the properties of a laminate. The characteristics of the first stripline structure are based on a split between the properties of the laminate and those of the prepreg material. The second stripline structure is dominated by the properties of the two laminates.

It is possible that a laminate can have a lower coefficient of thermal expansion (CTE) than a prepreg, which can affect a circuit’s performance in terms of reliability over temperature—the lower CTE providing enhanced reliability compared to a stripline construction with higher CTE. Prepreg materials also tend to exhibit higher electrical losses than laminates, which can be a consideration for stripline circuits in which minimizing loss is critical. There are also circuit fabrication yield issues, where sometimes one of these two methods will have much better circuit yields than the other.

In forming these multilayer circuits, it should be pointed out that the term prepreg actually refers to a wide variety of bonding materials, each with their own sets of features and capabilities. A prepreg is usually a thermoset material (where heat is the curing agent) which has woven-glass reinforcement. But some prepreg bonding materials are also available without support (without the woven-glass reinforcement), and these offer their own sets of benefits and challenges.

The table offers a comparison of common bonding materials with a subjective rating of different concerns. The comments listed for ease of fabrication, soldering, and reliability are based on various issues. Ease of fabrication, for example, is related to the lamination cycle, PTH processing, drilling required for forming PTHs, and the capability to endure multiple lamination cycles. Robust soldering is mostly related to multiple lead-free solder reflow cycles. Reliability is related to a material’s CTE, its decomposition temperature (T_d), PTH capabilities, thermal cycle testing, and high-layer-count capabilities.

To examine a somewhat more complex multilayer microwave PCB construction, consider a five-layer PCB with a combination of stripline and two microstrip circuit layers. The structure’s top and bottom layers are microstrip, while the inner layers will form the stripline circuit. There are a number of ways to fabricate this circuit, but the first approach detailed here will be the most cost-effective method. In this approach, the stripline circuitry is fabricated as in the method of Fig. 1. Then layers of prepreg and copper foils are added to the top and bottom of that initial stripline circuit, to achieve the five-layer circuit construction shown in Fig. 4. Because of the amount of prepreg used, this construction approach is dominated by the properties of the prepreg material. But there are numerous other methods for fabricating this five-layer microwave PCB, as shown in Fig. 5.

The fabrication process shown in Fig. 5(a) is used mainly for applications requiring cost-effective production, although its strong dependence on the properties of the prepreg material may also impact a choice of using this approach. The approach shown in Fig. 5(b) might be used in a case where the performance of the microstrip circuits was more critical than that of the stripline circuit. This is because the control of thickness of a copper-clad laminate is typically better than that of a prepreg-foil lamination at a circuit fabricator. In addition, extremely low-loss copper-clad laminates are available for the top and bottom microstrip circuit layers, making it possible to achieve outstanding performance for those layers compared to the stripline circuit layer.
The approach shown in Fig. 5(b) also supports the possibility of improved component assembly reliability. Again, copper-clad laminates can be selected for these outside microstrip circuit layers with low CTE values that are closely matched to copper or to the components being attached to these outside layers. During the soldering process, there is the inevitable expansion and contraction of the circuit-board material. If the CTE of the PCB material on the outer layers is high, there will be more mechanical stress on the solder joints—both during cooling and after the solder has solidified—which can degrade the reliability of the circuit assembly.

The approach shown in Fig. 5(c) might be suitable for an application where the performance of the stripline circuit must be as good as possible. Good stripline circuit performance can be achieved by using low-loss copper-clad laminates with a minimal amount of prepreg material to create the inner layers of the circuit structure. Also, if the performance of the outer microstrip circuit layers is not critical, there can be some cost benefits by fabricating these outer layers by means of copper foil and prepreg.

Finally, the approach shown in Fig. 5(d) supports applications where the properties of the copper-clad laminates are most required. Of course, these are just a handful of possible circuit fabrication methods, with many others possible depending upon a circuit designer’s creativity, along with the mechanical and electrical requirements of the circuit application.

In the original stripline circuit example and the two approaches presented to fabricate the circuit, it should be apparent that stripline in these cases cannot be formed into a truly homogeneous circuit. An exception might be a case where the prepreg layer exhibited the same properties as the laminate, although this is typically not the case.

Fortunately, methods are available to form a “pure package” stripline circuit by using specific circuit materials and fabrication techniques. This is done by using a copper-clad laminate based on polytetrafluorethylene (PTFE) dielectric material. PTFE is a thermoplastic which can melt and flow at higher processing temperatures. To build a homogeneous stripline circuit, the inner conductive layer circuit would be etched as before, and then another copper-clad PTFE-based laminate would have all of the copper removed from one side. These materials would then be joined together and laminated in a fusion process in which the PTFE substrates would melt, reflow together, and bond together upon cooling. If this process is followed carefully, a true homogeneous stripline circuit can be made. However, few circuit fabricators are capable of supporting this manufacturing method.

In forming these simple multilayer microwave PCBs, a number of different electrical issues can be encountered which are related to the choice of PCB materials, such as loss. The insertion loss of a stripline or microstrip circuit, for example, can be affected by the surface roughness of a copper layer. In general, the amount of loss is a function of the amount of roughness, with greater amounts of copper surface roughness resulting in higher amounts of insertion loss.

If the amounts of copper surface roughness are known, they can be included in computer circuit models. In the case of copper-clad laminates, the surface roughness of the copper is often known. But the copper surface roughness of copper foils used in some multilayer microwave circuits can vary widely.

For the example stripline circuit of Fig. 1, the manufacturer of the copper-clad laminate should be able to provide information on those two substrate-copper interfaces in terms of copper surface roughness. But information may be sketchy at best about the other two substrate-copper interfaces resulting from the copper foils. Even if the manufacturer of the copper foil knows the surface roughness of the foil, the top surface of the signal layer may have received a bond enhancement to its surface, which can alter the roughness. For the alternative method of building this stripline circuit (Fig. 3), three of the four copper-substrate interfaces could be known from the laminate supplier, but the top surface of the signal layer could still be unknown.

The choices of prepreg materials are many, and such a choice can especially impact the performance of stripline circuits with edge coupling or differential-pair stripline constructions. The prepreg would have a greater influence
on stripline circuits fabricated with the first example approach, where a greater amount of prepreg material is used, than in the alternative stripline circuit fabrication approach. Additionally, the type of bonding material used for edge coupled stripline circuits could have different effects on circuit performance due to the material’s woven-glass reinforcement. If the spacing between the conductors is relatively wide and the conductors are somewhat tall (using 1-oz copper or more), the prepreg will be between the edge-coupled conductors. The type of glass reinforcement used in the prepreg can have an effect on the electrical performance of the construction. For such a circuit design, it might be advantageous to fabricate the stripline using the alternative method (of Fig. 3) with a bonding material, such as FEP, that does not have woven-glass reinforcement.

The five-layer construction depicted in Fig. 4 can pose problems for achieving good grounding. The two buried ground planes must be maintained at precisely the same electrical potential. This is essential for achieving consistent and predictable stripline performance by minimizing parallel-plate inductances which can result from ground planes at unequal potential. Not only must the two buried ground planes be connected electrically, but they must also have a reliable connection to the outside ground plane. As a result, an abundant application of PTHs to connect not only the buried ground planes together, but also the buried ground planes to the outside ground plane, can ensure consistent stripline performance. The use of redundant PTHs placed on a close pitch can ensure reliable and repeatable ground connections in this type of five-layer stripline PCB structure.

Multilayer microwave PCBs can provide tremendous savings in volume for systems that are tight on space, but designing and fabricating such PCBs is fraught with numerous challenges. High-frequency circuit designers should utilize the experience of knowledgeable circuit fabricators and circuit materials suppliers to achieve the best results when designing and fabricating multilayer microwave PCBs. It is always recommended that the materials, circuits, and assemblies which are intended for a particular application are well tested for proper functionality in the intended application, both for short- and long-term considerations.